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ADA10001S3C

Linear Amplifier MMIC
Data Sheet - Rev. 1

FEATURES

- High Linearity (IIP_3 + 18 dBm)
- Low Noise Figure (2.0 dB)
- Single Supply (+8Vdc)
- Wide Bandwidth (50MHz - 1 GHz)

APPLICATIONS

- Driver Amplifier
- CATV - Distribution / Drop Amplifiers

S3C
16 Pin SOIC Package

DESCRIPTION:

The ADA10001 is a monolithic IC intended for use in applications requiring high linearity such as: Cellular Telephone Base Station Driver Amplifiers, CATV Fiber Receiver/Distribution Amplifiers and CATV Drop Amplifiers. Supplied in a surface mount, 16 lead-SOIC package, it is well suited for use in amplifiers where small size, reduced component count, and high reliability are important.

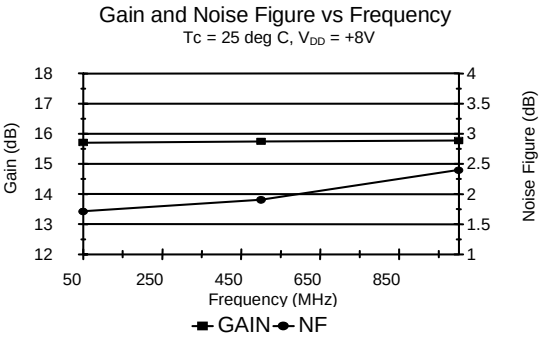
ABSOLUTE MAXIMUM RATINGS

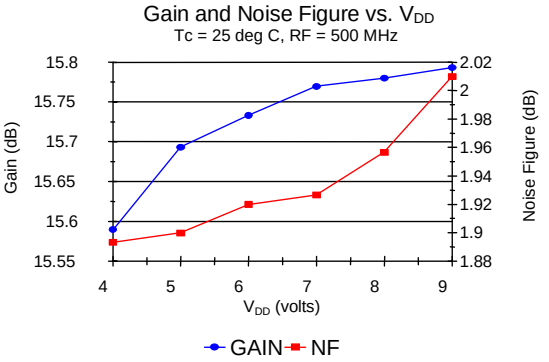
PARAMETER	MIN.	MAX.	UNITS
V_{DD}/ V_{RFOUT}	0	12	V_{DC}
V_{RFIN}		0	V_{DC}
RF_{IN}		+ 10	dBm
Storage Temperature	- 65	+150	°C
Soldering Temperature		260	°C
Soldering Time		5.0	Sec.
Thermal Resistance		35	°C/W

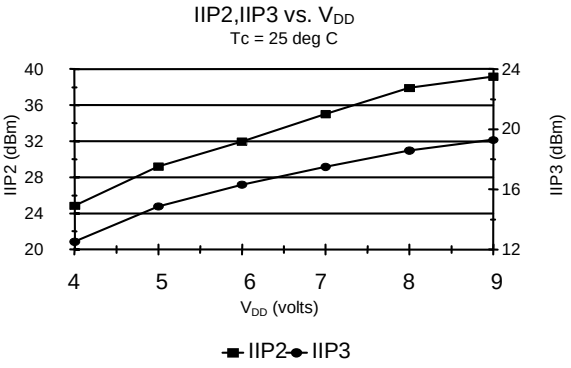
ELECTRICAL SPECIFICATIONS (T_A = +25 °C, RF = 50 to 1000 MHz, Test System = 75Ω, V_{DD} = + 8V_{DC})				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNITS**
CSO[2]	60			dBc
CTB[2]	65			dBc
Gain	14	15		dB
Noise Figure		2.0	3.5	dB
2nd Order Input Intercept Point (IIP2)[3]	+35	+38		dBm
3rd Order Input Intercept Point (IIP3)[3]	+15	+18		dBm

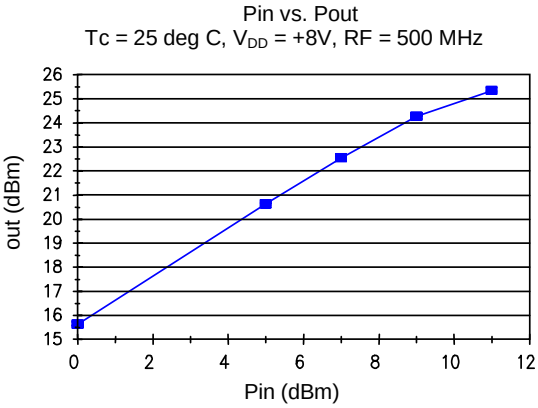
1. The device can be operated at + 6 V_{DC} for lower power dissipation; Refer to the figures on page 3 for performance variation with supply voltage.
2. 160 channels, + 23 dBmV per channel, (measured at the output) 6 MHz channel spacing.
3. Two tones, - 10 dBm per tone at input.

OPERATING RANGES				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNITS**
V_{DD}	4	8[1]	9	Volts
I_{DD}	50	-	150	mA
Case Temperature	-40	-	70*	°C



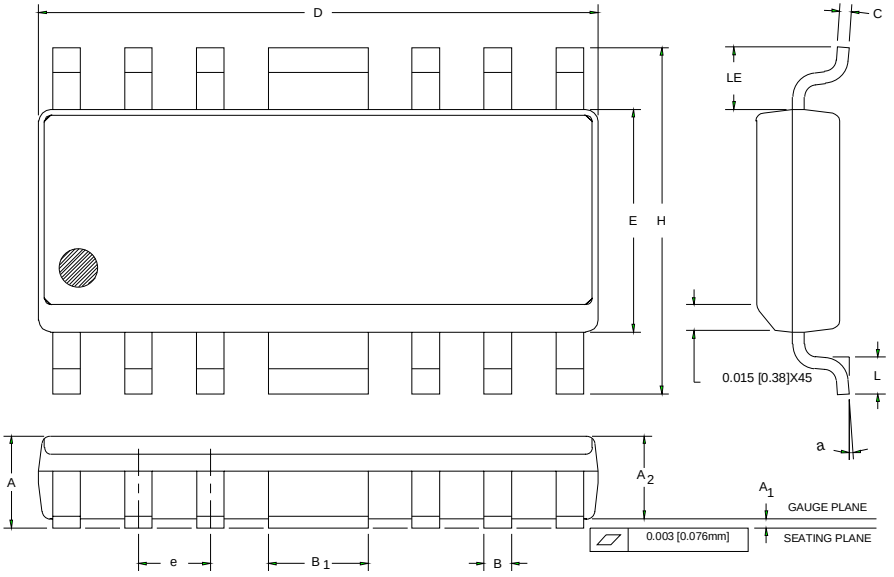






* Notes:

- IIP2 Measured at 986.5 MHz, Input = two tones (55.25 MHz and 931.25 MHz) at - 10 dBm.
- IIP3 Measured at 986.5 MHz, Input = two tones (986.5 MHz and 992.5 MHz) at - 10 dBm.



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A_1	0.004	0.010	0.10	0.25	
A_2	0.055	0.065	1.40	1.65	
B	0.013	0.020	0.33	0.50	
B_1	0.062	0.070	1.58	1.78	
C	0.008	0.010	0.20	0.25	4
D	0.380	0.400	9.66	10.16	2
E	0.150	0.160	3.81	4.06	3
e	0.050 BSC		1.27 BSC		
H	0.226	0.244	5.74	6.20	
L	0.016	0.040	0.41	1.02	
LE	0.030	—	0.76	—	
a	0	8	0	8	

NOTES:

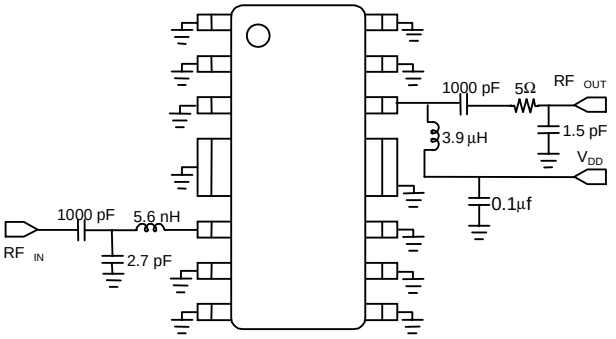
1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.

SPECIFICATION: 98000-006

SUBJECT: PUBLISHED OUTLINE, 16 LEAD BATWING SOIC PKG.

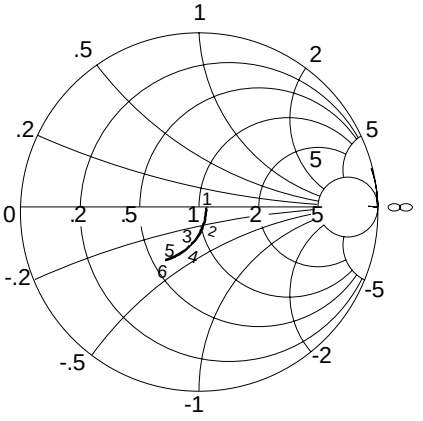
EXTERNAL TEST CIRCUIT

PIN FUNCTION	
1	GND
2	GND
3	NC
4	GND
5	GND
6	RF IN
7	NC
8	GND
9	GND
10	NC
11	NC
12	GND
13	GND
14	RF OUT
15	NC
16	GND



INPUT IMPEDANCE

START: 0.050 GHz
STOP: 1.00 GHz



1: 0.050 GHz
79.76 Ω
- 4.79 jΩ

2: 0.20 GHz
77.88 Ω
- 13.21 jΩ

3: 0.40 GHz
70.02 Ω
- 21.83 jΩ

4: 0.6 GHz
59.63 Ω
- 26.56 jΩ

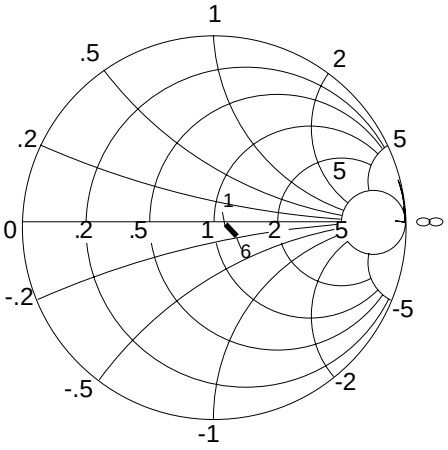
5 : 0.8 GHz
49.91 Ω
- 26.56 jΩ

6: 1.0 GHz
41.77 Ω
- 25.15 jΩ

Measured in 75 Ω System

OUTPUT IMPEDANCE

START: 0.050 GHz
STOP: 1.00 GHz



1: 0.050 GHz
83.9 Ω
- 8.1 jΩ

2: 0.20 GHz
84.17 Ω
- 1.19 jΩ

3: 0.40 GHz
85.38 Ω
- 2.27 jΩ

4: 0.6 GHz
87.64 Ω
- 3.82 jΩ

5 : 0.8 GHz
90.20 Ω
- 6.60 jΩ

6: 1.0 GHz
93.57 Ω
- 11.76 jΩ

Measured in 75 Ω System

NOTES

NOTES

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